handle the trickle of data flowing between the various devices residing within the computer system. However, as the demand for increased amounts of data skyrocket, designers have to find ways to improve the speed at which bits of data can be conveyed (i.e., increased bandwidth) over the bus. One such solution is to implement a switching matrix as described in the patent application entitled "Packet Switched Router Architecture For Providing Multiple Simultaneous Communications," Serial No. 08/717580, now 6,683,876 filed on September 23, 1996, and assigned to the assignees of the present invention. Rather than having a shared bus arrangement, a central "switchboard" arrangement is used to select and establish temporary links between multiple devices. In this manner, multiple links can be established between any number of components. In order to transmit data more efficiently within the scope of this new bus architecture, data is divided and transmitted in the form of "packets." These packets are then sent over the links. By selecting and establishing multiple links, the central switchboard allows multiple packets to be sent to various destinations. This results in significantly greater bandwidth because multiple high-speed packetized transmissions can occur simultaneously. In addition, such a packetized router architecture facilitates the implementation of a guaranteed bandwidth scheme (see patent application entitled "A Guaranteed Bandwidth Method In A Computer System For Input/Output Data Transfers," Serial No. 08/717581, now 5,764,569 filed on September 20, 1996, and assigned to the assignees of the present invention).

With the basic architecture and protocol established, there yet remains other unique, novel features which can be leveraged to gain even greater